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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,430	11/14/2003	Craig Hansen	43876-148	9134

20277   7590   12/05/2006

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EXAMINER
COLEMAN, ERIC

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 14-39,55-84 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 14-26,55-69 are directed to a computer readable medium having instructions that cause a computer to perform operations. The disclosure of the instant application discloses a computer readable medium comprising a transmission medium. Claims 27-39,70-84 are directed to a computer data signal embodied in a transmission medium the computer data signal having instructions that cause a computer to perform operations. These claims are directed to a medium or signal. A signal is not in any of the statutory classes of invention (namely machine manufacture, composition of matter, process). Note: the transmission of signals via air is a natural phenomenon. The signal is merely energy that is transmitted via a medium. The results or operations attributed of the claimed signal are not realized without use means that are not claimed (namely at least means for some type of receipt and decoding of the signal and means to perform the claimed operations). The instructions are not stored on a medium and that would provide access by a processor for properly timed operation to perform the claimed operations. The instructions are not embodied in a manner so as to be tangible. The instructions are merely portions of a medium or signal and these are not embodied so as to be tangible. Therefore the claims are not statutory (e.g., see MPEP 706.03(a)).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees.   A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-13,40-54 are provisionally rejected on the ground of nonstatutory double patenting over claims 1-13,26-3⁄ of copending Application No. 10/705946. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: claim 1 of the instant application and claim 1 of 10/705946 are presented side by side below:

10/705946	10/ 712430
1. A programmable processor comprising: an instruction path; a data path; and external interface operable to receive data from an external source and communicate the received data over the data path;	1. A data processing system comprising; (a) bus coupling components in the data processing system (b) an external memory coupled to the bus (c) a programmable microprocessor coupled to the bus capable of independent operation of another host processor, the microprocessor comprising virtual memory addressing unit; and instruction path and data path, an external interface operable to receive data from an external source and communicate the received data over the data path; a
a cache operable to retain communicated between the external interface and the data path; a register file operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction	cache operable to retain data communicated between the external interface and the data path; at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and an execution unit

10/705946	10/712430
and data paths and operable to decode and execute the instructions received from the instruction path,	coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction specifying both a shift amount and a register having a register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width, the execution unit operable to: : (i) shift a subfield of each of the first plurality of data elements by the shift amount to
wherein in response to decoding a single instruction specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width, the execution unit operable to: (i) shift a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data	

10/705946

elements; and (ii) provide the second plurality of data elements as a concatenated result.

10/712430

produce a second plurality of data elements; and (ii) provide the second plurality of data elements as a concatenated result.

As can been seen by the side by side display of claims 1 of the instant application and SN705946 both claims are directed to the same inventive concept. The differences comprise feature that would have been obvious to one of ordinary skill considering the features in the claims of SN 10/705946. The bus , external interface , external memory and implementing the processor as a microprocessor while including a virtual memory addressing unit a having the microprocessor capable of operation independent of another host are features one of ordinary skill would have been motivated to incorporate in the implementation of the claim 1 of SN 10/705946. The motivation for implementing the processor as microprocessor would have been to reduce system size and cost taking advantage of advances in the microprocessor technology at the time of the claimed invention. Further the motivation use of a bus external interface at least for accessing external memory would have been at least to allow the system to access large amounts of data and instructions or programs then could be stored internal to the microprocessor allowing for reduced cost of memory (bus using slower external memory). Also since the claim addressed data elements in width smaller than the width of the register and shifts were used to access the data elements. Then one of ordinary skill would have been motivated to address the data elements using virtual addressing via a virtual addressing unit to allow addressing more data elements than the system would have provided to address single each register.

Claims 2-13 of the instant application are word for word the same as corresponding

claims 2-13 of SN 10/705946 consequently these claims also are obvious in view of the

corresonponding claim of SN 10/705946.

Note the claims 40,45,50 of the instant application is directed to the same inventive

concept a claim 31 of SN 705946. Note claim 40,45 and 50 of the instant application is

directed to the same inventive concept as claim 26 of SN 10/705946. The differences

between the claims 40,45,50 in this application and claims 26,31 of SN 10/705946

comprises the bus, external memory and microprocessor   limitations which were

differences in claim 1 and the motivation for incorporating these features are the same

as for claim 1 described above. Further claims 41-44,46-49,51-54, are worded the same

are as claims 27-30, 32-35 of SN 10/705946 and therefore theses claims also are

directed to the same inventive concept as the corresponding claim in SN 10/705946.

Response to Arguments

Applicant's arguments with respect to claims 1-84 have been considered but are

moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eric Coleman whose telephone number is (571) 272-

4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER